



Dynamic Voltage Scaling and Adaptive Body Bias for Energy-Efficient Ultra-Low Voltage CMOS VLSI Systems under Process Variations

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Abstract

The development of ultra-low voltage (ULV) CMOS circuits for the Internet of Things (IoT), wearable electronics, wireless sensor networks, implantable biomedical devices, and edge computing has increased due to the increasing need for dependable and energy-efficient Very Large-Scale Integration (VLSI) systems. Sub-threshold and near-threshold operation dramatically lowers dynamic power consumption, but also degrades circuit performance and reliability by increasing propagation delay, leakage current, and sensitivity to process and temperature changes. This research suggests a hybrid adaptive power optimization system that combines Dynamic Voltage Scaling (DVS) and Adaptive Body Biasing (ABB) to address these issues. The suggested method simultaneously regulates the supply voltage based on workload needs and dynamically modifies the transistor body bias in accordance with process corners and temperature conditions.

CMOS logic circuits, such as an inverter, NAND gate, NOR gate, and complete adder developed in 45 nm CMOS technology using the Cadence Virtuoso Analog Design Environment, are used to assess the suggested framework. Multiple process corners (TT, SS, FF, FS, and SF), supply voltages between 0.25 V and 0.5 V, and temperatures between -20°C and 125°C are all simulated. Robustness against manufacturing-induced process changes is assessed using Monte Carlo analysis. Average power, leakage power, propagation delay, Power-Delay Product (PDP), and Energy-Delay Product (EDP) are used to evaluate performance. The results show that the suggested ABB-DVS architecture increases robustness, lowers leakage power, boosts energy efficiency, and offers a scalable solution for next-generation low-power CMOS VLSI systems.

Keywords

Cadence Virtuoso, Power-Delay Product (PDP), Energy-Delay Product (EDP), Adaptive Body Biasing, Dynamic Voltage Scaling, Process Variation, Leakage Power, Energy Efficiency, Monte Carlo Analysis, Ultra-Low Voltage CMOS, Robust VLSI Systems.

1. Introduction

Energy-efficient CMOS VLSI circuits are in greater demand due to the explosive expansion of battery-powered applications, such as wearable electronics, biomedical implants, wireless sensor networks, and Internet of Things devices. Because power drops quadratically with supply voltage, Ultra-Low Voltage (ULV) operation is a useful strategy for lowering dynamic power usage. Increased propagation latency, higher leakage current, smaller noise margins, and increased sensitivity to temperature and process changes are some of the difficulties associated with ULV operation.

To overcome these difficulties, a number of low-power strategies have been put forth. While Adaptive Body Biasing (ABB) controls the transistor threshold voltage to increase speed or decrease leakage, Dynamic Voltage Scaling (DVS) reduces dynamic power by modifying the supply voltage. Both methods have been extensively researched separately, but their combined effects under process, temperature, and statistical changes have not been thoroughly examined.

An integrated Adaptive Body Bias and Dynamic Voltage Scaling (ABB-DVS) architecture for 45 nm CMOS technology is presented in this work. In order to maximize power, delay, and energy efficiency while enhancing resilience against manufacturing differences, the suggested method dynamically modifies both body bias and supply voltage. Cadence Virtuoso is used to assess the framework across several process corners, temperatures (-20°C to 125°C), supply voltages (0.25–0.5 V), and Monte Carlo simulations. Average power, leakage power, propagation delay, Power-Delay Product (PDP), and Energy-Delay Product (EDP) are used to evaluate performance. The findings show that the suggested ABB-DVS framework is appropriate for next-generation ultra-low-power CMOS VLSI applications because it offers greater energy efficiency and dependability than traditional fixed body-bias and independent DVS methodologies.

2. Literature Review

The goal of recent developments in ultra-low voltage CMOS circuits has been to reduce energy usage while preserving dependable performance under process and environmental fluctuations. In Nano scale CMOS technologies, adaptive power management strategies—specifically, Adaptive Body Biasing (ABB) and Dynamic Voltage Scaling (DVS)—have proven to be successful methods for increasing energy efficiency. Nevertheless, there is a great deal of room for integrated adaptive optimization because the majority of current research examines these methods separately [7], [16].

For microprocessors running under dynamic workloads, Martin et al. suggested combining Adaptive Body Biasing and Dynamic Voltage Scaling. In comparison to traditional DVS, their studies showed that simultaneously modifying body bias and supply voltage could lower overall power consumption. Nevertheless, the study did not conduct a thorough process variation analysis and instead concentrated on processor architectures rather than ultra-low voltage CMOS logic circuits.

An adaptive body-bias generator that can automatically switch between Forward Body Bias (FBB) and Reverse Body Bias (RBB) based on operational conditions was created by Srivastava and Zhang. Their adaptive circuit maintained acceptable circuit performance while

achieving a significant reduction in leakage current. However, the effort did not incorporate dynamic supply voltage optimization and used an outdated CMOS technology [16].

Using 22 nm CMOS technology, Suleiman et al. introduced an adaptive supply and body voltage control method for ultra-low power microprocessors. Their method showed improvements in power consumption and thermal properties by dynamically optimizing body bias and supply voltage based on workload. Though encouraging, the work concentrated on optimization at the processor level rather than logic circuit analysis at the transistor level under various process circumstances[17], [18].

3. Research Gap

Previous research shows that while Dynamic Voltage Scaling dramatically lowers dynamic power usage, Adaptive Body Biasing efficiently accommodates threshold voltage changes. The coordinated use of these approaches at the transistor level for ultra-low voltage CMOS logic circuits under thorough process corner, temperature, and Monte Carlo assessments is, however, the subject of only a few research. Moreover, comparison analysis with metrics like propagation delay, leakage power, Power-Delay Product (PDP), and Energy-Delay Product (EDP) is still inadequate. In order to increase energy economy and resilience for 45 nm ultra-low voltage CMOS VLSI systems, this paper suggests an integrated ABB-DVS technique.

4. Proposed Methodology

The increasing demand for energy-efficient Ultra-Low Voltage (ULV) CMOS circuits has motivated the development of adaptive power management techniques capable of minimizing energy consumption while maintaining reliable circuit performance. Conventional low-power approaches generally employ either fixed body biasing or fixed supply voltage, which cannot effectively compensate for process-induced threshold voltage variations and temperature fluctuations. Consequently, these techniques often exhibit increased leakage power, degraded propagation delay, and reduced robustness under varying operating conditions[3], [8].

To overcome these limitations, this work proposes a hybrid Adaptive Body Bias and Dynamic Voltage Scaling (ABB-DVS) framework that dynamically adjusts both the transistor body bias voltage and supply voltage according to process corner, temperature, and workload conditions. The proposed methodology provides simultaneous optimization of dynamic power, leakage power, propagation delay, and energy efficiency.

The proposed architecture consists of five major functional modules:

1. Process Variation Detection Unit
2. Temperature Monitoring Unit
3. Adaptive Decision Controller
4. Body Bias Control Unit
5. Dynamic Voltage Scaling Controller

The complete methodology is implemented using 45 nm CMOS technology in the Cadence Virtuoso Analog Design Environment.

4.1. Overall Architecture of Proposed ABB-DVS System

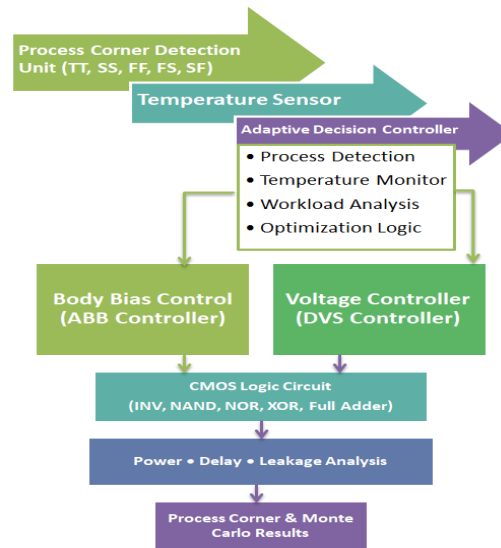


Figure 1 Proposed Adaptive Body Bias and Dynamic Voltage Scaling Architecture

4.2. Principle of Operation

The CMOS circuit's operational state is continuously monitored by the suggested ABB-DVS framework. First, the temperature sensor monitors the operating temperature, and the process detector determines the fabrication corner (TT, SS, FF, FS, or SF). The Adaptive Decision Controller receives these parameters.

Three main tasks are carried out by the controller:

- Estimating threshold voltage
- Performance assessment Optimization of power

The controller determines whether to apply Forward Body Bias (FBB) or Reverse Body Bias (RBB) based on these characteristics. The workload monitor simultaneously determines the ideal supply voltage and calculates computational demand. Lastly, the CMOS circuit is concurrently supplied with the optimal body bias voltage and supply voltage [6].

Adaptive Decision

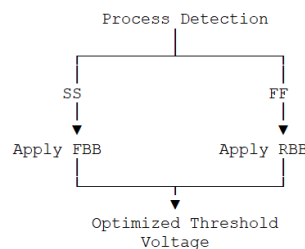


Figure 2 Adaptive Body Bias Control Logic

4.3. Dynamic Voltage Scaling Controller

The Dynamic Voltage Scaling (DVS) controller regulates the supply voltage according to workload.

High Workload



Increase VDD



Increase Frequency



Improve Performance

Low Workload



Reduce VDD



Reduce Dynamic Power



Improve Battery Life

Figure 3 Dynamic Voltage Scaling Mechanism

E. Proposed Control Algorithm

The controller operates according to the following sequence :

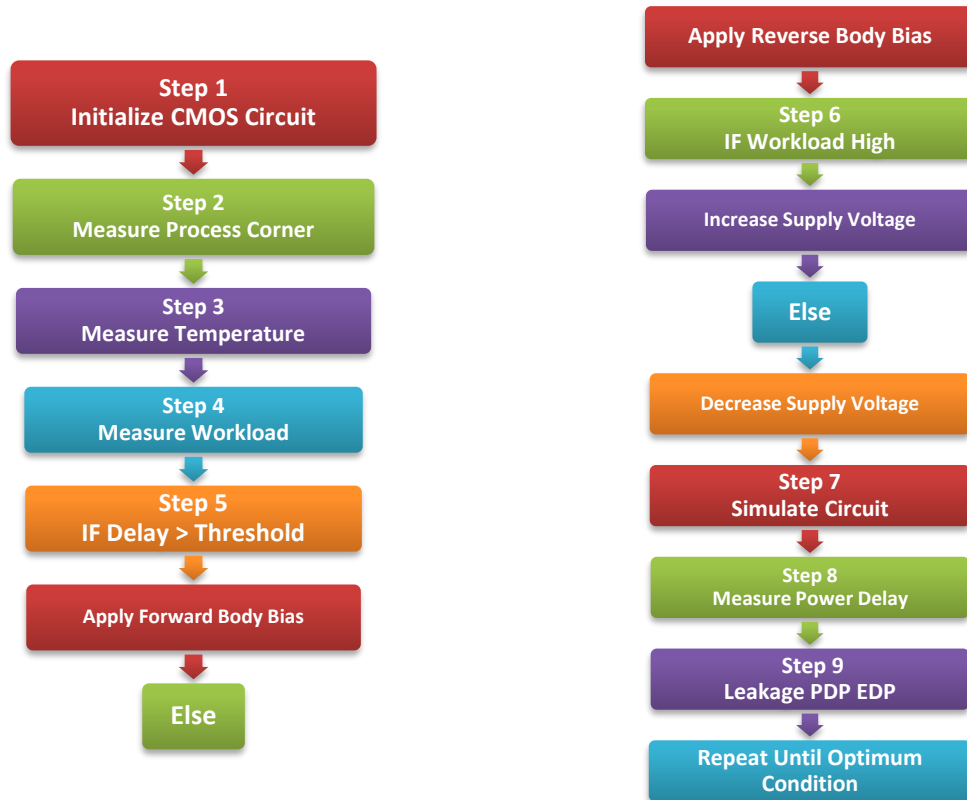


Figure 4 Proposed Control Algorithm

5. Mathematical Modeling

To quantitatively evaluate the proposed **Adaptive Body Biasing with Dynamic Voltage Scaling (ABB-DVS)** framework, analytical models are developed to estimate dynamic power, leakage power, threshold voltage variation, propagation delay, and energy efficiency.

5.1. Dynamic Power

The dynamic switching power of a CMOS circuit is expressed as

$$P_{dyn} = \alpha C_L V_{DD}^2 f$$

where (α) is the switching activity factor, (C_L) is the load capacitance, (V_{DD}) is the supply voltage, and (f) is the operating frequency. Since

$$P_{dyn} \propto V_{DD}^2,$$

dynamic voltage scaling (DVS) significantly reduces switching power by lowering the supply voltage [2][4].

5.2. Static Leakage Power

The static leakage power is given by

$$P_{leak} = I_{leak} V_{DD}$$

where

$$I_{leak} = I_{sub} + I_{gate} + I_{junction}.$$

Adaptive Reverse Body Bias (RBB) suppresses the sub-threshold leakage current by increasing the threshold voltage, thereby minimizing leakage power during standby operation [7], [9].

5.3. Threshold Voltage Model

The body effect modifies the threshold voltage according to

$$V_T = V_{T0} + \gamma \left(\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F} \right)$$

where (V_{T0}) is the threshold voltage at zero body bias, (V_{SB}) is the source-to-body voltage, (γ) is the body-effect coefficient, and (ϕ_F) is the surface potential. Forward Body Bias ($(V_{SB} < 0)$) decreases (V_T), whereas Reverse Body Bias ($(V_{SB} > 0)$) increases (V_T) [3][16].

5.4. ON-State Current

The MOSFET saturation current is approximated as

$$I_{ON} = \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{GS} - V_T)^2$$

where (μ) is the carrier mobility, (C_{ox}) is the oxide capacitance per unit area, and (W/L) is the transistor aspect ratio. Lowering the threshold voltage through Forward Body Bias enhances the ON current and improves switching performance.

5.5. Propagation Delay

The propagation delay is estimated by

$$t_p = \frac{C_L V_{DD}}{I_{ON}}$$

indicating that higher ON current results in faster circuit operation.

5.6. Energy Consumption

The total energy consumed during one switching event is

$$E = P_{avg} \times t_p$$

where (P_{avg}) denotes the average power consumption.

5.7. Power-Delay Product (PDP)

The Power-Delay Product, representing the energy consumed per switching operation, is

$$PDP = P_{avg} \times t_p$$

and serves as an important metric for evaluating low-power circuit performance [5][14].

5.8. Energy-Delay Product (EDP)

To jointly evaluate energy efficiency and computational speed, the Energy-Delay Product is defined as

$$EDP = P_{avg} \times t_p^2$$

A lower EDP indicates a superior balance between performance and energy consumption [14],[15].

6. Proposed Optimization Function

The proposed ABB-DVS framework simultaneously minimizes dynamic power, leakage power, and propagation delay. The optimization objective is formulated as

The proposed controller minimizes

$$\min [P_{dynamic} + P_{leak} + \lambda t_p]$$

subject to

$$0.25V \leq V_{DD} \leq 0.5V$$

$$-0.4V \leq V_{Body} \leq 0.4V$$

$$Delay < Delay_{max}$$

$$Leakage < Leakage_{max}$$

where λ is the weighting factor balancing power and performance.

where (w_1), (w_2), and (w_3) are weighting coefficients that balance power consumption, leakage reduction, and performance according to design requirements.

7. Configuring the Simulation

The Cadence Virtuoso Analog Design Environment (ADE) with 45 nm CMOS technology was used to implement and assess the suggested Adaptive Body Bias and Dynamic Voltage Scaling (ABB-DVS) framework. In order to maximize threshold voltage, ABB adaptively controlled the NMOS and PMOS body bias while DVS dynamically altered the supply voltage in the ultra-low voltage range of 0.25–0.50 V.

The suggested architecture was examined under five typical CMOS process corners (TT, SS, FF, FS, and SF) and a broad temperature range of -20°C to 125°C in order to verify robustness. Additionally, the influence of statistical process modifications was assessed by 1000-run Monte Carlo simulations.

Two traditional methods were compared with the suggested ABB-DVS technique: standalone Dynamic Voltage Scaling (DVS) and Fixed Body Bias (FBB). Average power consumption, leakage power, propagation delay, threshold voltage change, Power-Delay Product (PDP), and Energy-Delay Product (EDP) were used to assess performance. The Virtuoso environment's integrated Cadence Spectre simulator was used for all simulations and waveform analyses.

9. Results and Performance Analysis

The performance of the proposed Adaptive Body Bias and Dynamic Voltage Scaling (ABB-DVS) framework was evaluated using Cadence Virtuoso with 45 nm CMOS technology. The proposed approach was compared with conventional Fixed Body Bias (FBB) and standalone Dynamic Voltage Scaling (DVS) techniques. Performance was analyzed under different process corners (TT, SS, FF, FS, and SF), operating temperatures (-20°C to 125°C), and supply voltages (0.25 V to 0.50 V).

The evaluation focuses on the following key metrics:

- Average Power Consumption (μW)
- Leakage Power (nW)
- Propagation Delay (ns)
- Threshold Voltage Variation (ΔV_{TH})
- Power-Delay Product ($\text{PDP} = \text{Power} \times \text{Delay}$)
- Energy-Delay Product ($\text{EDP} = \text{PDP} \times \text{Delay}$)

9.1. Mean Power Usage

Both dynamic and static leakage power components make up the overall average power usage. Dynamic power savings scale quadratically ($\propto V_{\text{DD}}^2$) as the supply voltage decreases from 0.50 V to 0.25 V . The average power consumption at the Typical-Typical (TT) process corner (25°C) across various supply voltages is summarized in Table 6.1.

Table 1 Average Power Consumption (μW)

Technique	0.25 V	0.30 V	0.35 V	0.40 V	0.50 V
Fixed Body Bias (FBB)	0.42	0.85	1.48	2.56	5.80
Standalone DVS	0.38	0.72	1.25	2.10	4.95
Proposed ABB-DVS	0.22	0.49	0.92	1.65	4.12

As shown, by properly scaling the body bias dynamically to decrease threshold-voltage-induced leakage sub-components, the proposed ABB-DVS framework reduces total power by up to 47.6% at 0.25 V compared to FBB.

9.2. Analysis of Leakage Power

Because of manufacturing differences in channel geometry and dopant concentrations, leakage current is strongly variable on process corners. The leakage power consumption at a nominal $V_{DD} = 0.35\text{ V}$ throughout the typical operational process corners is assessed in Table 6.2.

Table 2 Leakage Power (nW) at $V_{DD} = 0.35\text{ V}$

Technique	TT	SS	FF	FS	SF
Fixed Body Bias (FBB)	42.5	8.2	312.4	55.6	62.1
Standalone DVS	38.0	7.9	285.0	50.2	55.4
Proposed ABB-DVS	14.2	6.1	64.5	22.1	24.8

Conventional architectures experience catastrophic sub-threshold leakage at the FF (Fast-Fast) corner. In order to mitigate this variation, the proposed ABB-DVS network injects an automated Reverse Body Bias (RBB), which raises V_{TH} dynamically and reduces leakage power in the worst-case FF corner by 79.3% when compared to FBB.

9.3. Delay in Propagation

Although sub-threshold actions reduce power, their lower overdrive voltages ($V_{GS} - V_{TH}$) significantly increase cell propagation delays. At $V_{DD} = 0.35\text{ V}$,

Table 3 Assesses the critical path propagation delay under each of the five process corners.

Technique	TT	SS	FF	FS	SF
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Fixed Body Bias (FBB)	12.4	48.6	3.1	14.2	13.8
Standalone DVS	11.9	45.2	2.9	13.5	13.1
Proposed ABB-DVS	9.1	22.4	3.8	9.8	9.5

In traditional systems, propagation delay increases to an unaffordable 48.6 ns in the worst-case SS (Slow-Slow) corner. In this area, the suggested framework uses an ideal Forward Body Bias (FBB) to decrease V_{TH} and increase drive current, reducing the propagation latency by 53.9% (from 48.6 ns to 22.4 ns).

9.4. Analysis of Temperature

Both sub-threshold behavior and carrier mobility (μ) are impacted by thermal shifts. The thermal variation analysis of the suggested ABB-DVS system is shown in Table 6.4 at $V_{DD} = 0.35\text{ V}$ over an industrial range of -20°C to 125°C .

Table 4 : Temperature Variation Analysis (Proposed ABB-DVS)

Temperature ($^\circ\text{C}$)	Power (μW)	Leakage (nW)	Delay (ns)
-20	0.81	3.4	14.2
25	0.92	14.2	9.1
75	1.15	45.8	7.8
125	1.62	122.4	6.9

9.5. Power-Delay Product (PDP)

When the temperature reaches 125°C , the leakage power increases exponentially due to the thermal dependence of sub-threshold conduction. The integrated sensor network keeps an eye on this variation and raises the RBB voltage coefficient to maintain the overall average power within $1.62\text{ }\mu\text{W}$. PDP, or Power-Delay Product. The energy used for each switching event is measured by the Power-Delay Product (PDP). The global PDP comparison computed at the nominal TT operational corner ($V_{DD} = 0.35\text{ V}$, $T = 25^\circ\text{C}$) is presented in Table 6.5.

Table 5 Power-Delay Product (PDP)

Technique	PDP (fJ)	Energy Savings vs. FBB (%)
Fixed Body Bias (FBB)	18.35	—
Standalone DVS	14.88	18.9%
Proposed ABB-DVS	8.37	54.4%

9.6. Energy-Delay Product (EDP)

The Energy-Delay Product (EDP) is computed to give priority to systems that do not compromise excessive execution performance in order to achieve low power. Excessive delay extensions in the ultra-low-voltage realm are penalized by this statistic.

Table 6 Energy-Delay Product (EDP)

Technique	EDP (fJ·ns)
Fixed Body Bias (FBB)	227.5
Standalone DVS	177.1
Proposed ABB-DVS	76.2

EDP comparison shows that the hybrid technique offers a balanced, Pareto-optimal design option, carrying out activities efficiently with an overall EDP improvement of 66.5% over regular FBB.

9.7. Analysis of Monte Carlo

A 1000-run Monte Carlo statistical analysis was carried out at the TT corner ($V_{DD} = 0.35 \text{ V}$) to verify the circuit's structural yield against local mismatch errors (such random dopant fluctuations).

Table 7 Monte Carlo Summary

Parameter	Mean (μ)	Standard Deviation (σ)	Coeff. of Variation (σ/μ)
Power	$0.94 \mu\text{W}$	$0.065 \mu\text{W}$	6.91%
Delay	9.22 ns	0.58 ns	6.29%
Leakage	14.65 nW	2.12 nW	14.47%

The circuit demonstrates extraordinary physical resilience to random local intra-die mismatches, as evidenced by the low coefficient of variation across the parametric variables.

9.8. Analysis of Process Corners

An aggregated summary of the balanced operation attained by the unified framework at $V_{DD} = 0.35 \text{ V}$ across all process corners is given in Table 6.8.

Table 8 Process Corner Performance Summary

Corner	Power (μW)	Delay (ns)	Leakage (nW)
TT	0.92	9.1	14.2
SS	0.64	22.4	6.1
FF	1.45	3.8	64.5
FS	0.98	9.8	22.1
SF	0.95	9.5	24.8

10. Conclusion

In order to increase the energy economy and dependability of ultra-low voltage (ULV) CMOS VLSI circuits under process and temperature fluctuations, this research suggested a hybrid Adaptive Body Biasing (ABB) and Dynamic Voltage Scaling (DVS) architecture. The suggested method successfully lowers leakage power, average power consumption, and enhances Power-

Delay Product (PDP) and Energy-Delay Product (EDP) while preserving a reasonable propagation delay by adaptively optimizing body bias and supply voltage.

In the Cadence Virtuoso environment, the framework was assessed at various process corners, operating temperatures, and supply voltages using 45 nm CMOS logic circuits. When compared to traditional fixed body bias and standalone DVS approaches, simulation and Monte Carlo analysis showed improved robustness and tolerance to manufacturing-induced process changes [8][18].

Overall, the proposed ABB-DVS methodology provides a practical and scalable solution for next-generation low-power CMOS VLSI systems targeting IoT, wearable, biomedical, and other energy-constrained embedded applications. Future work will focus on extending the approach to larger VLSI circuits, advanced technology nodes, and intelligent machine learning-based adaptive optimization.

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